

WHAT IS CLAIMED IS:

1 1. A circuit comprising:
2 a domain-synchronizing controller which produces a source
3 enable signal based on a synchronous pulse signal, the source
4 enable signal enabling a source register to capture data from
5 a source domain; and

6 a source-enable controller which produces a source
7 inhibit signal, the source inhibit signal controlling the
8 production of the source enable signal by the domain-
9 synchronizing controller.

1 2. The circuit in claim 1, wherein the source-enable
2 controller produces the source inhibit signal until the data
3 is available at the source register.

1 3. The circuit in claim 1, wherein the source-enable
2 controller produces the source inhibit signal based on a ratio
3 between a source domain clock and a destination domain clock.

1 4. The circuit of claim 3, wherein the source enable
2 controller comprises:

3 an event detector which monitors a source event signal
4 and the source enable signal; and

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5 a counter which counts the ratio between a source domain
6 clock and a destination domain clock.

1 5. The circuit in claim 3, wherein the source enable
2 controller produces a source input select signal to control
3 the selection of the data from a plurality of source
4 registers.

1 6. The circuit in claim 1, further comprising a
2 destination enable controller which produces a destination
3 inhibit signal, the destination inhibit signal preventing the
4 domain-synchronizing controller from producing a destination
5 enable signal, the destination enable signal enabling a
6 destination register to capture the data at a destination
7 domain.

1 7. The circuit in claim 1, wherein the domain-
2 synchronizing controller comprises:

3 a plurality of flip-flops connected in a loop, the
4 plurality of flip-flops including a first flip-flop operating
5 at a source clock frequency and a second flip-flop operating
6 at a destination clock frequency; and

7 a first logic component positioned between two of the
8 plurality of flip-flops, the first logic component inverting

9 the output of a prior flip-flop before reaching the input of a
10 next flip-flop to produce the synchronous-pulse signal.

1 8. The circuit in claim 7, wherein the source inhibit
2 signal controls a second logic component to prevent the
3 domain-synchronizing controller from propagating the
4 synchronous pulse signal.

1 9. The circuit in claim 7, wherein the second logic
2 component is a multiplexor.

1 10. The circuit in claim 8, further comprising a third
2 logic component positioned between an input and an output for
3 the first flip-flop, the second logic component producing the
4 source enable signal.

1 11. The circuit in claim 10, further comprising a fourth
2 logic component positioned between an input and an output for
3 the second flip-flop, the fourth logic component producing a
4 destination enable signal.

1 12. The circuit in claim 10, wherein the third logic
2 component is an XOR gate.

1 13. A circuit comprising:

2 a plurality of flip-flops connected in a loop, the
3 plurality of flip-flops including a first flip-flop operating
4 on a source domain clock and a second flip-flop operating on a
5 destination domain clock;

6 a first logic component positioned within the loop, the
7 first logic component inverting the output of one of the flip-
8 flop to produce a synchronous-pulse signal which propagates
9 through the plurality of flip-flops; and

10 a second logic component receiving an inhibit signal, the
11 second logic component preventing the propagation of the
12 synchronous-pulse signal based on the inhibit signal.

1 14. The circuit in claim 13, wherein the first logic
2 component is an inverter and the second logic component is a
3 multiplexor.

1 15. The circuit in claim 13, further comprising a third
2 logic component positioned between an input and an output to
3 the first flip-flop, the first logic component producing a
4 source enable signal.

1 16. The circuit in claim 15, wherein the third logic
2 component is an XOR gate.

1 17. The circuit in claim 13, further comprising a third
2 logic component positioned between an input and an output for
3 the second flip-flop, the third logic component producing a
4 destination enable signal based on the input and the output to
5 the second flip-flop.

1 18. A method of transferring data between a source
2 domain and a destination domain, the method comprising:
3 producing a source-enable signal based on a synchronous-
4 pulse signal, the source-enable signal enabling a source
5 register to capture data from a source domain; and
6 controlling the source-enable signal with a source-
7 inhibit signal, the source inhibit signal preventing the
8 synchronous-pulse signal from producing the source-enable
9 signal until the data is available for transmission.

1 19. The method in claim 18, further comprising producing
2 the source-inhibit signal based on a ratio between a source
3 domain clock and a destination domain clock.

1 20. The method in claim 18, further comprising producing
2 the source-inhibit signal until the data is available at the
3 source register or based on a ratio between a source domain

4 clock and a destination domain clock, whichever produces the
5 source inhibit signal for a longer duration.

1 21. The method of claim 18, further comprising:
2 monitoring a source-event signal; and
3 producing a source-input select signal which controls the
4 selection of the data from a plurality of destination
5 registers.

1 22. The method in claim 18, wherein producing the
2 source-enable comprises:
3 operating a plurality of flip-flops in a loop, the
4 plurality of flip-flops including a first flip-flop operating
5 at a source domain clock and a second flip-flop operating at a
6 destination domain clock;
7 inverting an output of a prior flip-flop before reaching
8 an input of a next flip-flop to produce the synchronous-pulse
9 signal; and
10 preventing a propagation of the synchronous-pulse signal
11 through the plurality of flip-flops based on the source
12 inhibit signal.

1 23. The method in claim 22, further comprising
2 originating the synchronous pulse signal before the first
3 flip-flop or the second flip-flop based on a selection signal.

1 24. A circuit to drive a domain register, comprising:
2 a first logic component which receives a source enable
3 signal and an source inhibit signal;
4 a flip-flop which samples an output of the first logic
5 component based on an inverted signal of a domain clock; and
6 a second logic component which receives an output of the
7 flip-flop and the domain clock, the second logic component
8 producing a gated clock pulse to drive the domain register.

1 25. The circuit in claim 24, wherein the first and
2 second logic components are AND-gates and further comprising:
3 an inverter which inverts the source inhibit signal prior
4 to being received by the first logic component.

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